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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/635,703	08/05/2003	David B. Glasco	NWISP036	8389

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EXAMINER	
THOMAS, SHANE M	

ART UNIT	PAPER NUMBER
2186	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/635,703	GLASCO, DAVID B.	
	Examiner	Art Unit	
	Shane M. Thomas	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office action is responsive to the response filed 12/14/2005. Claims 1-20 remain pending.

Response to Arguments

Applicant's arguments with respect to claims 1-20 have been considered and are persuasive; the Examiner agrees with the characterization of the Sharma reference as argued by the Applicant and that the --remote data cache-- as defined by the Examiner does not properly reflect a --remote data cache-- as defined by the Applicant's specification (page 21, line 26 - page 22, line 2).

Applicant arguments with respect to claims 1-20, rejected under 35 U.S.C. 103(a) as obvious over Hum in view of Bauman, have been considered and are persuasive. However, the Examiner respectfully disagrees with the mischaracterization of the Applicant's arguments with regard to the Hum prior art reference. Applicant asserts that the processors of Hum are not connected in a point-to-point architecture but referring exclusively to Hum's figure 7 (page 6, ¶1 of the response). While the Examiner agrees that figure 7 does not show a point-to-point architecture, Hum states that figure 7 is just a single embodiment with which the present invention can be practiced (¶109) and further teaches that instead of multiple processors, a single processor can be considered a node. Further because the MESIF cache design is recursive and that the system of Hum can be practiced with any number of hierarchy layers (¶57, and ¶71-72) - such that a single cluster can comprise a single node and hence a single processor - it would have been obvious to one having ordinary skill in the art to have practiced the teachings of Hum with

a cluster representing a single processor (and therefore the processors would be connected in a point-to-point manner - ¶57) since Hum suggests that multiple different arrangement and hierarchies are contained in the scope of Hum's teachings - ¶71-72. Finally, Hum explicitly teaches that a point-to-point connection exists between nodes (¶57).

Applicant further argues on page 6, ¶2, of the response that a remote data cache "holds data from remote clusters" and that "any cache holding data from remote clusters accessed by local processors that is accessed after local caches but before a home cluster memory controller. The Examiner notes that such a limitation is not included in the independent claims, but Hum does teach such a "remote data cache" - as the combination of the import and export data caches 250/2660 as herein discussed.

As per the Applicant's successful arguments in light of the Bauman reference, the Examiner has modified the obviousness rejection under 35 U.S.C. 103 such that claims 1-7,11-17, and 20 are rejected as being unpatentable over Hum in view of Sharma as discussed below.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-7, 11-17, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hum et al. (U.S. Patent Application Publication No. 2004/0123047) in view of Sharma et al. (U.S. Patent No. 6,108,737).

As per claims 1, 11, and 20, Hum teaches a method for providing a response to a cache access request in figures 4 and 6. Further, Hum shows a *processing cluster* 110 in figure 1. Figure 4 shows the receiving of a cache access request [that is associated with a memory line] at a cache coherence controller (agent 120, figure 1). The cache coherence controller 120 represents multiple nodes, and cluster interface 210 (figure 2) provides two-way communication between the agent 120 and the set of nodes (¶76). Since Hum states that an agent represents multiple nodes (¶76), that a node can be comprised of a single processor (¶109), and that the cache coherency system of the present invention is scalable (¶71), the Examiner is considering elements 112-118 to be simple nodes (comprised of a single processor). Thus *cluster* 110 comprises cache coherence controller 120 and processor nodes 112-118. The processors of cluster 110 are interconnected in a point-to-point architecture through agent 120 (refer to ¶¶ 55, 57 and 76). Response information for the cache access can be obtained from remote data cache 250 (import data cache) in accordance to figure 4 or can be obtained from remote data cache 260

(export directory) in accordance to figure 6. Since figure 2 is a representation of an agent (cache coherence controller) is can be seen that remote data caches 250 and 260 are associated with a given agent. In accordance with figure 4, the agent provides response information (step 450) to the requesting node (processor).

A determination regarding whether the cache request can be handled locally by using a remote data cache 250 or 260 without having to probe remote nodes is taught by Hum in ¶67 and ¶105. Hum does not specifically teach in ¶67 or ¶105 that if the request is handled locally, that a completion response is provided with the response information (claim lines 10-11). Completion responses are well-known in the cache-coherency art to enable a requesting processor determine whether it must wait [for invalidating acknowledgements from other processors caching the data] in order to modify the requested data, thereby preserving data coherency among the processing cluster. Sharma teaches such a method when response information is sent from a cache coherency controller (in the case of Hum, the cache coherency controller is being considered the agent which acts and is seen as a processor/node - ¶58). Also, a completion indicator can be sent by a cache coherency controller - agent 120 (column 15, lines 54-59). Such a response is taught by Sharma as a type 0 commit-signal (column 15, lines 33-59).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have combined the cache coherency system of Hum with the completion response messaging system of Sharma in order to have minimized the latencies in delivering requested data to requesting processors. Such a benefit readily applies to the scenario regarding a processor requesting data for read modification purposes (i.e. a request that can be fulfilled by

the export cache [remote data cache 260]). It could have been seen that such a request would have received a response from the agent (cache coherency controller) with the C bit 310 (figure 3 of Sharma) [of modified Hum] set if no other Peer node contained the data, thereby indicating that no delayed purge will occur and the requesting processor can immediately modify the data. Without the completion response (type 0 commit-signal) indicating that no other processors currently cache a valid copy of the data, the requesting processor would have to wait for NACK - which are responses indicating that the respective processor does not have the requested memory address - messages to be returned from each of the Peer Nodes (¶66 of Hum), thereby slowing down the time until the requesting processor can utilize the data.

The messaging of modified Hum that contains the completion response also is similar to the ACK message of Hum (¶44). The ACK message is taught to indicate that the requested data has been sent to the requesting node.

Further regarding claims 11 and 20, the cache access request can be handled locally if a valid copy of the memory line is in the remote data cache as taught in figure 4 (steps 420-450) and figure 6 (steps 620-640) of Hum.

As per claim 2, the cache access request can be handled locally if a valid copy of the memory line is in the remote data cache as taught in figure 4 (steps 420-450) and figure 6 (steps 620-640) of Hum.

As per claims 3 and 13, Hum teaches in ¶43 that in the cache coherency system of the present invention, state information (M/E/F/S) can be included as part of the response information.

As per claims 4, as shown in figure 3 of Sharma --completion indicator-- is a

--completion bit-- (type 0 commit-signal or C bit 310), which designates whether an external probe is required (column 15, lines 33-59).

As per claims 5 and 15, if the --completion indictor-- is set in the response from the modified agent of Hum, it would indicate that the current response will be the only response from the agent (cache coherency controller) as taught in column 15, lines 33-59, of Sharma.

As per claims 6 and 16, the Examiner is considering the node (processor) requesting the data to be a --requesting processor-- (for instance processor 112, figure 2 of Hum), and the requesting processor's cluster (cluster 110) to be a --requesting cluster-- since the cluster comprised the processor from which a request for data initiated.

As per claims 7 and 17, as shown in figure 4, if the requested data is in the import cache (remote data cache) of the cache coherence controller, the data is forwarded to the requesting node (step 450). Only if the request misses in the remote data cache will the cache coherence controller (120) send the request to the nodes that are represented by the cluster (step 445). Further, the --completion indicator-- allows the cache coherence controller to avoid probing local or remote nodes when a data request (without write privileges) for data that is cached in the remote cache (250 or 260) occurs, as the cache coherency controller maintains the status of the requested data in local and remote nodes (¶66). The completion indicator is shown being set for a read request in column 15, lines 52-54, and column 9, lines 14-36.

As per claim 12, the Examiner is considering the data response message from the agent 120 (cache coherence controller) that is sent to a requesting node (processor) to be a --response packet-- that comprises the requested data and the state of the data (M/E/F/S) to be used by the requesting processor (¶43).

As per claim 14, Hum teaches that the response can include data (¶43).

Claims 8-10, 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hum et al. (U.S. Patent Application Publication No. 2004/0123047) in view of Sharma (U.S. Patent No. 6,108,737), as applied to claims 1-7, 11-17, and 20, above, in further view of Keller (U.S. Patent No. 6,728,841).

As per claims 8 and 18, modified Hum does not specifically teach the [requesting] processor sending a --source done-- upon identifying the completion indicator in the response from the cache coherency controller. Keller teaches in column 2, line 63 - column 3, line 11, that a step of sending a --source done-- upon receiving a response packet (including requested data) from a target node. The source done response would have allowed the target node to remove the request for data from its command queue and can proceed to process the next request for the memory location. As evidenced by Keller, the sending of the acknowledgement (source done) from the source node back to the target node allows a cache coherent multiprocessor system to process memory read requests effectively. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have combined the cache response method of Hum with the messaging response teaching of Keller in order to have effectively maintained cache-coherence during memory reads in the multiprocessing system of Hum (figure 1 for instance). It would have been seen by one having ordinary skill in the art that once the requesting node of modified Hum (source node of Keller) received the read response (containing requested data) followed by an type 1 message containing the PG_ACK bit (completion indicator) from the remote data cache (import cache 250) of the cache coherence controller

(agent 120), the requesting processor (node) would have sent a --source done-- response back to the cache coherence controller so that the cache coherence controller could have removed the read request from its command queue and to proceed to grant the subsequent read request.

As per claims 9 and 19, as discussed in the rejection for claims 8 and 18, the --source done-- message is sent to the cache coherence controller (agent 120).

As per claim 10, as discussed in the rejection for claims 8 and 18, the --source done-- response is sent back to the cache coherence controller (agent 120). The Examiner is considering the cache coherence controller to be --acting as a memory controller-- since it controls the read requests send to a node in its local cluster and can forward the data back to the requesting node without having to send the request to the target node (processor). Refer to ¶63 of Hum.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shane M. Thomas whose telephone number is (571) 272-4188. The examiner can normally be reached M-F 8:30 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt M. Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shane M. Thomas